Patent

Custom No.: 31561
Docket No.: 08727-US-PA
Application No.: 10/063,737

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Applicant	: Jimmy Hsu
Application No.	: 10/063,737
Filed	: 2002/5/9
For	: VOLTAGE REFERENCE CIRCUIT LAYOUT INSIDE MULTI-LAYERED SUBSTRATE
Art Unit	: 2825
Examiner	: Bowers, Brandon

TRANSMITTAL LETTER
002-1-703-872-9306
(Via fax : 1+7 pages)

Assistant Commissioner for Patents
Alexandria, VA 22314

Dear Sir,

In response to the Office Action dated February 23, 2005(Paper No.: 20050205), please find the Response to Office Action, in 7 pages.

I believe that no fee is incurred. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-2620 (Order No.: 08727-US-PA).

Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

Date : May 23, 2005

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	)	
Hsu	)	Examiner : BOWERS, BRANDON
	)	
Serial No. : 10/063,737	)	Art Unit : 2825
	)	
Filed : 05/09/2002	)	Docket No. : 8727-US-PA
	)	
For : VOLTAGE REFERENCE CIRCUIT LAYOUT INSIDE MULTI-LAYERED SUBSTRATE	)	

No fee is believed to be due. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-2620 (Order No. 8727-US-PA).

RESPONSE TO FINAL OFFICE ACTION

United States Patent and Trademark Office
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Mail Stop **AF**
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Dear Sir:

The Office Action mailed February 23, 2005 has been carefully considered. In response thereto, please enter the following amendment and consider the following remarks.

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In The Claims:

Claim 1-15 (Cancelled)

Claim 16. (Previously Presented) A multi-layered substrate having a voltage reference signal circuit layout therein, comprising:

at least one signal layer having a plurality of signal traces;

a non-signaling layer having a voltage reference signal trace, wherein the voltage reference signal trace is wider than the other signal traces; and

a conductive plane between the signal layer and the non-signaling layer.

Claim 17. (Original) The multi-layered substrate of claim 16, wherein the non-signaling layer includes at least one power plane.

Claim 18. (Original) The multi-layered substrate of claim 16, wherein the non-signaling layer includes at least one ground layer plane.

Claim 19. (Original) The multi-layered substrate of claim 16, wherein the non-signaling layer includes at least one power plane and a plurality of signal traces.

Claim 20. (Original) The multi-layered substrate of claim 16, wherein the non-signaling layer includes at least one ground layer plane and a plurality of signal traces.

Claim 21. (Original) The multi-layered substrate of claim 16, wherein the conductive plane includes a ground plane.

Claim 22. (Original) The multi-layered substrate of claim 16, wherein the conductive plane includes a power plane.

Claim 23-33 (Cancelled)

REMARKS

Present Status of the Application

The Office Action rejected presently-pending claims 16-22. Specifically, the Office Action rejected claims 16-22 under 35 U.S.C. 103(a), as being unpatentable over Sharma et al. (US 5,990,547) in view of Brooks et al. (US 6,326,244). Applicant respectfully requests reconsideration of those claims.

Discussion of Office Action Rejections

The Office Action rejected claims 16-22 under 35 U.S.C. 103(a), as being unpatentable over Sharma et al. (US 5,990,547) in view of Brooks et al. (US 6,326,244). Applicant respectfully traverses the rejections for at least the reasons set forth below.

Sharma does not teach, disclose or suggest the feature of "a non-signaling layer having a voltage reference signal trace" as claimed in claim 16. More specifically, as disclosed in column 3, lines 55-56 of Sharma, on which the Examiner relies to reject the present application, "... the layers 4 and 6 are voltage reference layers which in a specific embodiment include a ground layer and a power layer ...". Further, as shown in FIG. 3 and column 3, lines 62-64 of Sharma, "... The trace 28 in turn, is connected to a via 30 which makes contact with an isolated trace 32 at routing layer 4 ...". However, as described in column 3, lines 65-67, "... The trace 32 in turn makes contact with the via 34 which is a through hole via. The through hole via 34 makes contact to

both of the plating buses 36 and 38". That is, *the isolated trace 32 is used to connect plating buses to the traces going to be plated*, such as solder pad 16, 19, 51 or the bond posts 27 (column 3, lines 49-52). Accordingly, *the isolated trace 32 is not the voltage reference signal trace as claimed in claim 16 of the present invention*.

Contrary to the Office's assertion, neither Sharma nor Brooks teaches nor suggests that the voltage reference signal trace is wider than the other signal traces. Brooks simply discloses that the reference plane element reduces the self inductance through an increase in effective width and a decrease in the distance between the voltage reference plane and traces. Increasing the effective width of the reference plane element not necessary means that the width of the reference plane element is wider than other signal traces even the distance between the voltage reference plane and traces is decreased. It is possible that the width of the reference plane element and the width of other traces increases correspondingly. Further, the problem seeks to be solved by Brooks is different from the present invention. Therefore, the motivation to combine Sharma with Brooks is lacking.

Accordingly, even combined with Brooks, the **combination of Sharma and Brooks does not render claim 16 obvious** because Sharma does not teach, disclose or suggest "a non-signaling layer having a voltage reference signal trace" as claimed in claim 16. Therefore, claim 16 is patentable over Sharma in view of Brooks.

Accordingly, claims 17-22 are patentable over Sharma in view of Brooks as a matter of law since claim 16, which is depended by claims 17-22, is patentable over Sharma in view of Brooks.

For at least the foregoing reasons, Applicant respectfully submits that independent claim 16 patently defines over the prior art references, and should be allowed. For at least the same reasons, dependent claims 17-22 patently define over the prior art as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 16-22 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : May 23, 2005

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Registration No.: 46,863

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